IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of	Docket No.: P27144
Daniel C. EDELSTEIN et al.	Confirmation No.: 1995
Serial No.: 10/707,996	Group Art Unit: No. 2813
Filed: January 30, 2004	Examiner: L. M. Schillinger

For: **DEVICE AND METHODOLOGY FOR REDUCING EFFECTIVE DISLECTRIC CONSTANT IN SEMICONDUCTOR DEVICES**

REQUEST FOR PRE-APPEAL BRIEF REVIEW

Commissioner for Patents
U.S. Patent and Trademark Office
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Sir:

This request is being filed concurrently with a Notice of Appeal and is responsive to the Final Official Action of January 17, 2007.

Reconsideration and withdrawal of the 35 U.S.C. § 102(b) and the 35 U.S.C. § 103(a) rejections of claims 1-6 are respectfully requested in view of the arguments presented in the Rule 1.116 Response and the following remarks.

A prima facie case of anticipation has not been set forth and the Rejections Under 35 U.S.C. §§ 102(b) and 103(a) are improper

Examiner's Assertion

In rejecting claim 1 as anticipated by US Patent No. 6,358,813 to HOLMES et al., the Examiner identifies (see Advisory Action of April 3, 2007) Figs. 4-6 as disclosing forming a sub lithographic template mask over the insulator layer and selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect (claim 1).

Applicant's Response

Applicant disagrees. It is not disputed that Fig. 4 shows a silicon nitride hard mask 8

arranged over a silicon nitride stop layer 5, that the layer 8 is arranged over electrode 7, and that layer 5 is arranged over oxide 2a. Nor is it disputed that Fig. 6 shows that the layers 8 and 5 are removed by etching and that valleys 10a are formed by etching into the electrode 7 (see col. 3, lines 1-17). However, this is simply not the same as selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect (claim 1). First, although the Examiner argues that the silicon nitride stop layer 5 of HOLMES is properly interpreted as the recited insulator layer, the Examiner has failed to identify any language in HOLMES which supports the Examiner's position that the layer 5 is in fact an insulator layer. Nor has the Examiner identified any prior art document which explains that a silicon nitride stop layer 5 is *per se* an insulator layer. Second, because HOLMES discloses that both layers 8 and 5 are etched away (see col. 3, lines 16-17 and Fig. 6), it is not apparent that HOLMES teaches to selectively etch layer 5, which the Examiner has identified as the recited insulator layer. Third, because HOLMES etches both the silicon nitride hard mask 8 and the silicon nitride stop layer 5 during the formation of the valleys 10a in electrode 7, it is not understood how HOLMES can be properly interpreted to disclose selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect. The reasons are threefold:

(A) As is apparent from Fig. 6, the layer 5 is clearly not etched through the layer 8 to form the features 10a. Instead, the features 10a are formed in electrode 7 by etching through layer 8. The etching of the layer 5 does not participate in forming the features 10a, which are only formed in the interconnect 7 below layer 8 and in areas not covered by layer 5.

(B) Col. 3, lines 11-16 of HOLMES specifically makes clear that the so-called lithographic features 10a are formed by etching "only .. into the electrode material 7" (emphasis added). In HOLMES, no features are formed by etching an insulator layer, much less, by etching layer 5. Again, features 10a are only formed in the electrode 7 by etching layer 8.

(C) A proper interpreted claim 1 requires etching of the insulator layer through the sub lithographic template mask to form sub lithographic features in the insulator layer. Otherwise, the Examiner is ignoring the language of claim 1 which clearly recites that the insulator layer is provided with at least one interconnect, and that the sub lithographic features are formed so that

they span to a sidewall of the at least one interconnect. In contrast, a fair comparison 4-6 of HOLMES clearly shows that the features 10a are formed in the electrode 7, not in the so-called insulator layer 5. As no features are formed in layer 5 (or layer 2a for that matter), the features 10a cannot span to a sidewall of the at least one interconnect 7. Thus, in HOLMES, the features 10a are only formed in electrode 7 by virtue of etching layer 8, and are not formed in layer 5 by etching layer 5.

Examiner's Assertion

The Examiner identifies Fig. 15 of HOLMES as disclosing that the recited sub lithographic features are substantially vertical columns in the insulator layer (claim 2).

Applicant's Response

Applicant disagrees. The Examiner's rejection is improper for at least two reasons. First, the Examiner is basing an anticipation rejection of claim 2 on a combination of two different embodiments, i.e., the embodiment of Figs. 4-6 used to reject claim 1 and the alternative embodiment of Fig. 15 (see col. 2, lines 1-2 of HOLMES). While this may be proper in an obviousness rejection, this not proper in an anticipation rejection. Second, even accepting the Examiner's assertion that the silicon nitride stop layer 5 of HOLMES is properly characterized as the recited insulator layer, the Examiner must acknowledge that the so-called insulator layer 5 does not have any sub lithographic features, much less, ones which have the form of substantially vertical columns. Fig. 15, like Fig. 6, clearly shows that the so-called features 10a are formed in the electrode material 7, and not in the so-called insulator layer 5. Claim 2 specifically recites that the substantially vertical columns are in the insulator layer. In contrast, Fig. 15 of HOLMES shows the features 10a formed only in the electrode material 7.

Examiner's Assertion

The Examiner identifies Fig. 13 of HOLMES as disclosing that the sub lithographic features further include a plurality of holes formed in a capping layer beneath the sub lithographic template mask and having a diameter or cross section less than a diameter or cross section of the at least one interconnect and also substantially equal to the substantially vertical columns in the insulator layer (claim 3).

Applicant's Response

Applicant disagrees. The Examiner's rejection of claim 3 is improper for at least four

reasons. First, the Examiner is basing an anticipation rejection on a combination of two embodiments, i.e., the embodiment of Figs. 4-6 used to reject claim 1 and the alternative embodiment of Figs. 13 and 15 (see col. 2, lines 1-2 of HOLMES). Again, while this may possibly be proper in an obviousness rejection, this is not proper in an anticipation rejection. Second, the Examiner's assertion that Fig. 13 shows the recited capping layer is incorrect. It is true that Fig. 13 shows a silicon nitride hard mask 8 arranged over a silicon nitride stop layer 5, and that an oxide layer is arranged in the openings of the layer 8. However, to the extent that the oxide formed in the openings of layer 8 can be properly characterized as the recited capping layer, the Examiner must acknowledge that this oxide layer is clearly not beneath the sub lithographic template mask 8. Third, claim 3 requires that a plurality of holes are formed in a capping layer beneath the sub lithographic template mask. However, Fig. 13 clearly shows no features or holes formed in any layers. To the extent that layer 8 has holes, they are filled with the oxide, and vice versa. Layer 5 is also lacking in any features or holes. Fourth, Fig. 15 at most shows the features 10a formed only in the oxide layer and the electrode material 7. However, even in Fig. 15, no features or holes are shown formed in a capping layer beneath the sub lithographic template mask. To the contrary, Fig. 15 lacks the recited mask layer 8 and has no capping layer beneath it. To the extent that the oxide layer can be called the recited capping layer, (a) it is not beneath any layer, (b) it is certainly not beneath layer 8 (which has been removed in Fig. 15), and (c) layer 5 cannot be characterized as the recited capping layer 5 at least because it is not beneath layer 8 (which has been removed) and has no holes formed therein.

Examiner's Assertion

The Examiner identifies Fig. 10 of HOLMES as disclosing that the sub lithographic features are substantially vertical columns in the insulator layer and that the sub lithographic features further include a plurality of holes having a diameter less than a diameter of the at least one interconnect and substantially equal to the substantially vertical columns in the insulator layer and a top portion of the holes are tapered (claim 6).

Applicant's Response

Applicant disagrees. The Examiner's rejection is improper for at least two reasons. First, the Examiner's assertion that hexagon shaped holes (as shown in Fig. 10) are the same as holes whose top portions are tapered is without merit. Second, even accepting the Examiner's

assertion that the silicon nitride stop layer 5 of HOLMES is properly characterized as the recited insulator layer, the Examiner must acknowledge that the so-called insulator layer 5 does not have any sub lithographic features, much less, ones which have the form of substantially vertical columns. As explained above, Fig. 6, clearly shows that the so-called features 10a are formed in the electrode material 7, and not in the so-called insulator layer 5. As claim 6 specifically recites that the substantially vertical columns are formed in the insulator layer and as Fig. 6 of HOLMES shows the features 10a formed only in the electrode material 7 (not in the layer 5), this rejection is improper.

Examiner's Assertion

In support of the obviousness rejection of claim 5 over HOLMES alone, the Examiner explains that Applicant has admitted in the specification that the features of claim 5 are known.

Applicant's Response

This is incorrect for at least three reasons. First, the Examiner has failed to point to any language in the specification which supports the Examiner position that the features of claim 5 are admitted to be known. Second, claim 5 specifically recites that an undercut is formed below the at least one interconnect. All of the embodiments shown in HOLMES, however, show features 10a which do not extend to a position below the electrode material 7. As such, HOLMES clearly fails to disclose or suggest any undercuts formed below the at least one interconnect 7. Third, even if it were known to form undercuts beneath an interconnect, neither the specification nor HOLMES provide any reason or basis for melding together adjacent features 10a or for utilizing undercuts in the features 10a of HOLMES.

CONCLUSION

Reconsideration of the Final Office Action and allowance of the present application and all the claims therein are respectfully requested and now believed to be appropriate.

Respectfully submitted,
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